

## User's Guide

# **NHD-5.7-320240WFB-ETXI#** **LCM**

(Liquid Crystal Display Module)  
**RoHS Compliant**

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0	2008.04.01		First issue
A	2008.05.27	8	Modify pin2 and pin8

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# 1. Module Classification Information

NHD    5.7-320240 WFB - E T X I    #  
 ①                      ②                      ③    ④    ⑤ ⑥ ⑦                      ⑧

① Brand : NEWHAVEN DISPLAY INTERNATIONAL, LLC.

② Display Size: 5.7inch diagonal, 320xRGBx240 pixels

③ Display Type : WFB: TFT

④ Model serials number: **E : with Epson Controller**

⑤ Backlight Type :

N→Without backlight	A→LED, Amber
B→EL, Blue green	R→LED, Red
D→EL, Green	O→LED, Orange
W→EL, White	G→LED, Green
F→CCFL, White	<b>T</b> →LED, White
Y→LED, Yellow Green	S→LED, Bright White

⑥ LCD Mode :

B→TN Positive, Gray	T→FSTN Negative
N→TN Negative,	M→STN Negative, Blue
G→STN Positive, Gray	F→FSTN Positive
Y→STN Positive, Yellow Green	<b>X</b> : TFT, normally white

⑦ LCD Polarizer Type/ Temperature range/ View direction

A→Reflective, N.T, 6:00	H→Transflective, W.T,6:00
D→Reflective, N.T, 12:00	K→Transflective, W.T,12:00
G→Reflective, W. T, 6:00	C→Transmissive, N.T,6:00
J→Reflective, W. T, 12:00	F→Transmissive, N.T,12:00
B→Transflective, N.T,6:00	<b>I</b> →Transmissive, W. T, 6:00
E→Transflective, N.T.12:00	L→Transmissive, W.T,12:00

⑧ Special Code

**#** : RoHS Compliant

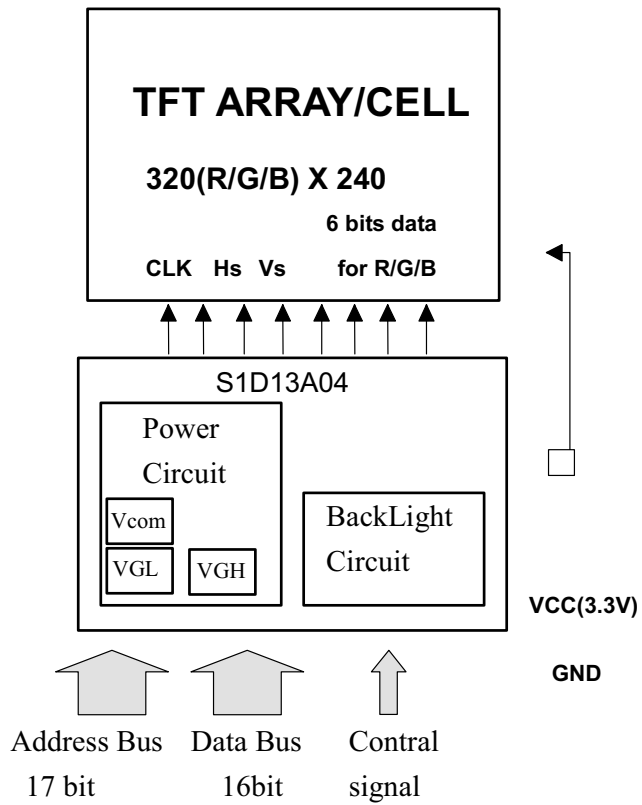
This product is composed of a TFT LCD panel, driver ICs, FPC, Control Board and a backlight unit.

Item	Dimension	Unit
Dot Matrix	320 x RGBx240(TFT)	dots
Module dimension	149.0x 109.0 x 11.5 (max)	mm
View area	115.200x 86.40	mm
Dot pitch	0.12 x 0.36	mm
Driving IC package	COG	
LCD type	TFT, Negative, Transmissive	
View direction	6 o'clock	
Backlight Type	LED, Normally White	
Controller IC	SID13A04 - 16 bit mode only	

\*Expose the IC number blaze (Luminosity over than 1 cd) when using the LCM may cause IC operating failure.

\*Color tone slight changed by temperature and driving voltage.

## 2. Block Diagram



Bit0 ~ Bit4 RED  
 Bit5 ~ Bit10 GREEN  
 Bit11~ Bit15 BLUE

### **3.Electrical Characteristics**

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VCC	—	3.0	3.3	3.6	V
Input High Volt.	V <sub>IH</sub>	—	0.7 V <sub>CC</sub>	—	V <sub>CC</sub>	V
Input Low Volt.	V <sub>IL</sub>	—	0	—	0.3V <sub>CC</sub>	V
LCD Driving Supply Voltage	V <sub>GH</sub> *1	Ta=25°C		15		V *3
	V <sub>GL</sub> *2			-10		V
	V <sub>comH</sub>		2.5		5.5	
	V <sub>comL</sub>		-2.0		0	
Supply Current	I <sub>VDD</sub>	V <sub>DD</sub> =3.3V	—	5	8	mA

Notes:

\*1) V<sub>GH</sub> is TFT Gate on operating Voltage.

\*2) V<sub>GL</sub> is TFT Gate off operating Voltage, V<sub>GL</sub> signal must be fluctuates with same phase as V<sub>com</sub> when Storage on Gate structure.

\*3) V<sub>com</sub> must be adjusted to optimize display quality\_Crosstalk, Contrast Ratio and etc.

### **4.Absolute Maximum Ratings**

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T <sub>OP</sub>	-20	—	+70	°C
Storage Temperature	T <sub>ST</sub>	-30	—	+80	°C
Power Supply Voltage	V <sub>GH</sub>	-0.3	—	18	V
	V <sub>GL</sub>	-15	—	0.3	V
	VCC	-0.3	—	6.0	V

## 5. Interface Pin Function

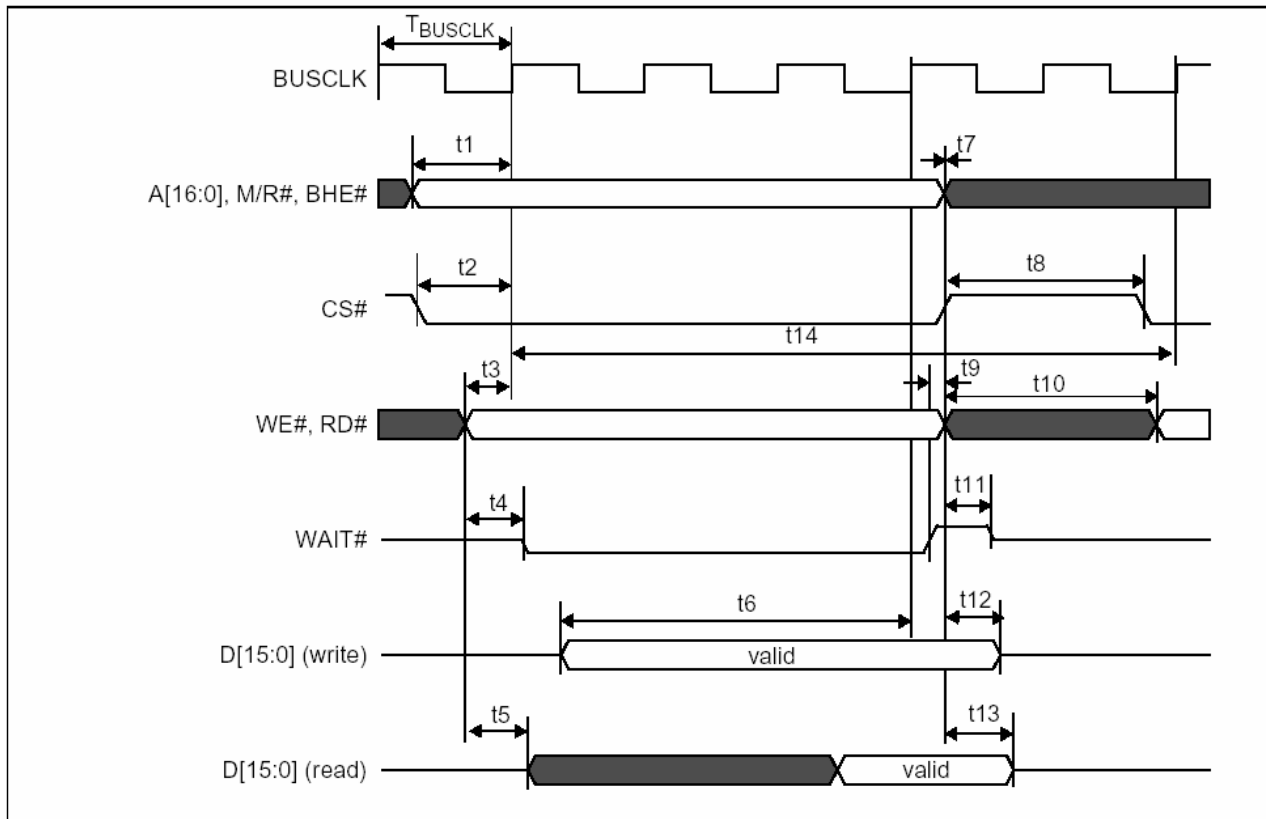
### 5-1 Pins Connection To Control Board

P/N	Symbol	Function	P/N	Symbol	Function
1	Vcc	Power Supply : +3.3V	26	VCC	Power Supply : +3.3V
2	Vcc	Power Supply : +3.3V	27	CLK	Typically used as input clock source for pixel clock . Normally this pin can be floated
3	DB0	Input data from the system data bus.	28	GND	Ground for logic circuit
4	DB1		29	GND	Ground for logic circuit
5	DB2		30	GND	Ground for logic circuit
6	DB3		31	AD1	System address bus bits
7	DB4		32	GND	Ground for logic circuit
8	DB5		33	AD2	System address bus bits
9	DB6		34	GND	Ground for logic circuit
10	DB7		35	AD3	System address bus bits
11	DB8		36	GND	Ground for logic circuit
12	DB9		37	AD4	System address bus bits
13	DB10		38	AD5	
14	DB11		39	AD6	
15	DB12		40	AD7	
16	DB13		41	AD8	
17	DB14		42	AD9	
18	DB15	43	AD10		
19	CS	Chip select input.	44	AD11	
20	MR	See Note(1)	45	AD12	
21	RD	this pin inputs the read command	46	AD13	
22	WR	write enable signal	47	AD14	
23	BHE	This pin inputs the byte enable signal for the high data byte *Note (2)	48	AD15	
24	REST	Active low input to set all internal registers to the default state	49	AD16	
25	WAIT	This pin outputs the wait signal	50	AD17	

Note(1): M/R# is set high to access display buffer, low to access the registers.

Note(2): BHE should be set LOW, this display supports Little Endian 16-bit mode only.

## 6. Timing Characteristics



### 6-1. Interface Timing

Symbol	Parameter	Min	Max	Unit
$f_{\text{BUSCLK}}$	Bus clock frequency		50	MHz
$T_{\text{BUSCLK}}$	Bus clock period	$1/f_{\text{BUSCLK}}$		ns
t1	A[16:0], M/R#, BHE# setup to first BUSCLK rising edge where CS# = 0 and either RD# = 0 or WE# = 0	9		ns
t2	CS# setup to BUSCLK rising edge	9		ns
t3	RD#, WE# setup to BUSCLK rising edge	1		ns
t4	RD# or WE# state change to WAIT# driven low	1	10	ns
t5	RD# falling edge to D[15:0] driven (read cycle)	2	10	ns
t6	D[15:0] setup to 4th rising BUSCLK edge after CS#=0 and WE#=0	1		$T_{\text{BUSCLK}}$
t7	A[16:0], M/R#, BHE# and CS# hold from RD#, WE# rising edge	0		ns
t8	CS# deasserted to reasserted	0		ns
t9	WAIT# rising edge to RD#, WE# rising edge	0		ns
t10	WE#, RD# deasserted to reasserted	1		$T_{\text{BUSCLK}}$
t11	Rising edge of either RD# or WE# to WAIT# high impedance		0.5	$T_{\text{BUSCLK}}$
t12	D[15:0] hold from WE# rising edge (write cycle)	2		ns
t13	D[15:0] hold from RD# rising edge (read cycle)	1		ns
t14	Cycle Length	6		$T_{\text{BUSCLK}}$

## 7. Optical Characteristics

Ta=25±2°C, ILED=140mA

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Tr	$\theta=0^\circ$	-	15	30	ms	Note 3,5
	Tf		-	35	50	ms	
Contrast ratio	CR	At optimized viewing angle	150	200			Note 4,5
Color Chromaticity	White	$\theta=0^\circ$	(0.25)	(0.30)	(0.35)		Note 2,6,7
			(0.27)	(0.32)	(0.37)		
Viewing angle	Hor.	CR≥10	50	65	-	Deg.	Note 1
			50	65	-		
	Ver.		30	50	-		
			50	55	-		
Brightness	-	-	300	350	-	cd/m <sup>2</sup>	Center of display

## 7.1 Definition of optical characteristics

Note 1: Definition of viewing angle

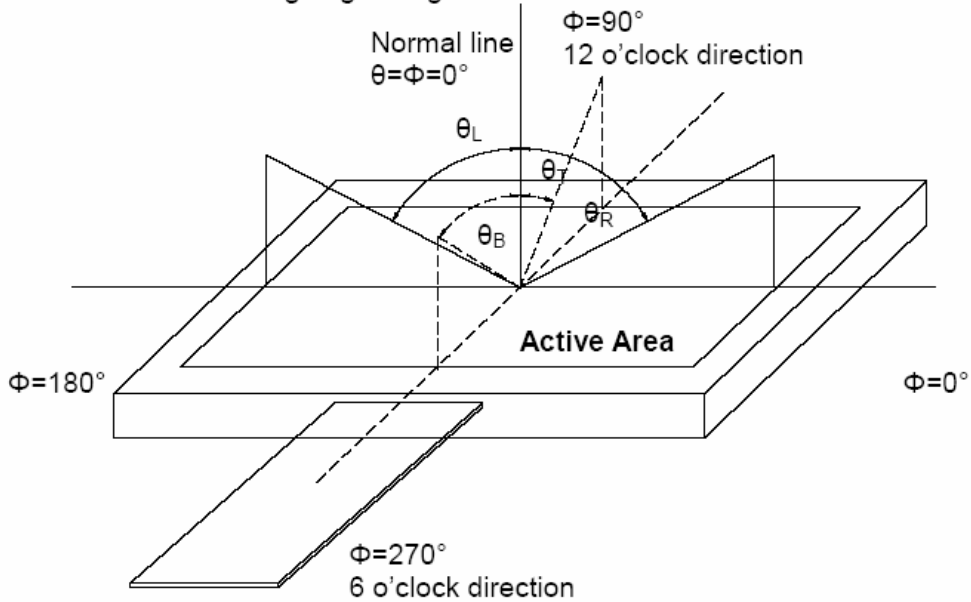


Fig. 5-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view:  $1^\circ$  /Height: 500mm.)

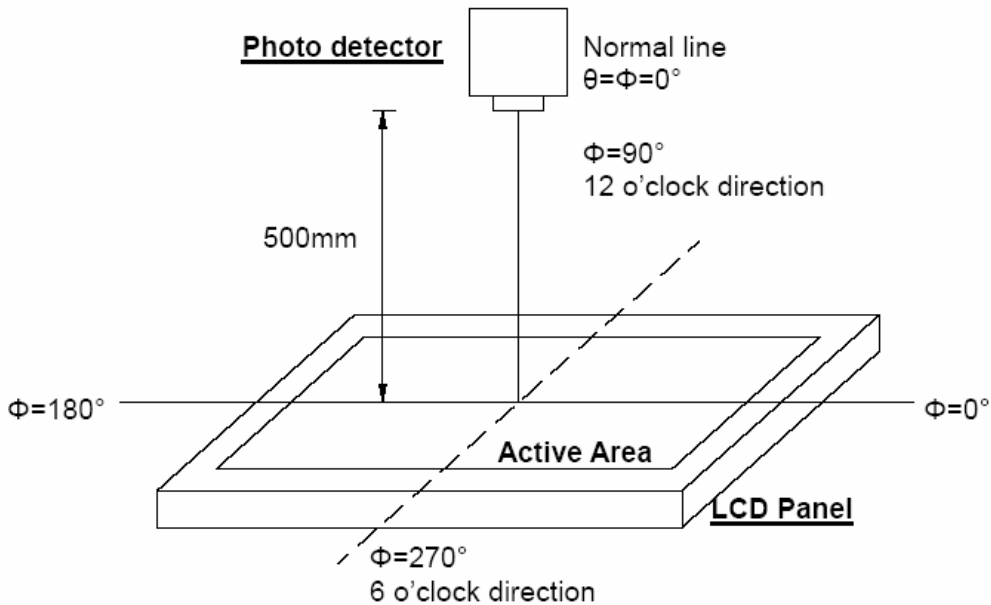


Fig. 5-2 Optical measurement system setup

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Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time ( $T_{ON}$ ) is the time between photo detector output intensity changed from 90% to 10%. And fall time ( $T_{OFF}$ ) is the time between photo detector output intensity changed from 10% to 90%.

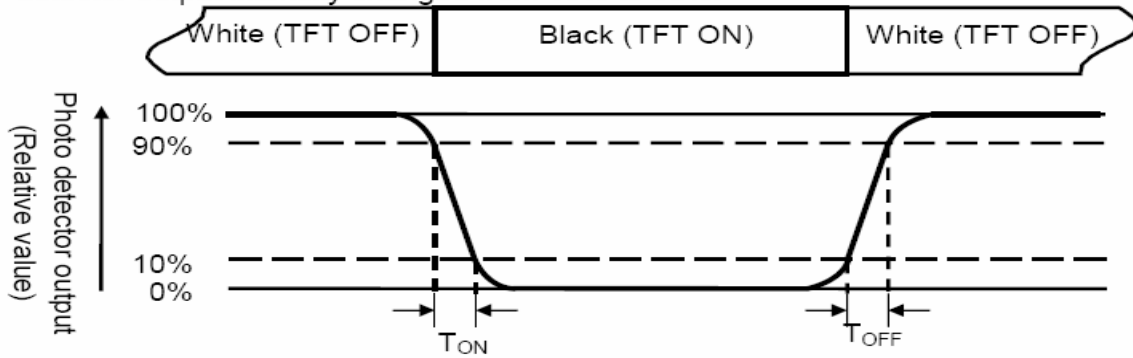


Fig. 5-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground when measuring the center area of the panel.

Note 7: Definition of Luminance Uniformity

To test for uniformity, the tested area, which is inside the active area, is divided into 3 rows and 3 columns. The measurement spot is placed at the center of each box.

$$\text{Luminance Uniformity (Yu)} = \frac{B_{min}}{B_{max}}$$

L-----Active area length      W----- Active area width

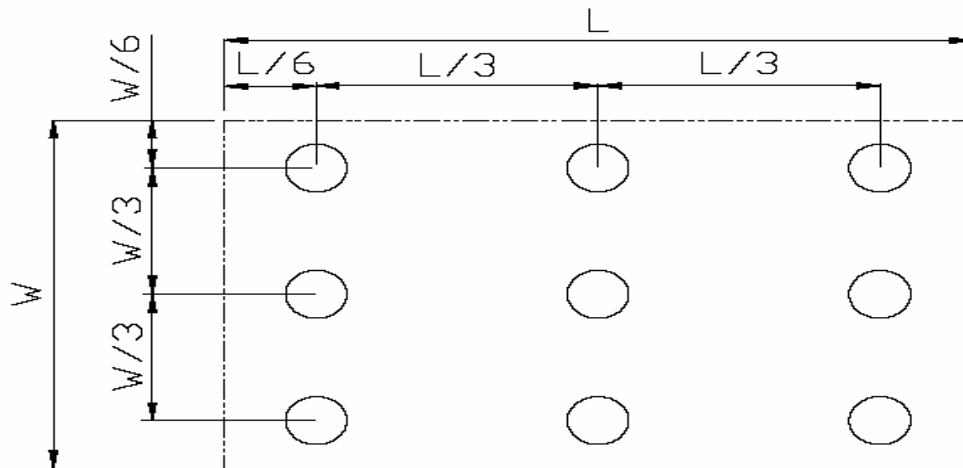


Fig. 5-4 Definition of uniformity

$B_{max}$ : The measured maximum luminance of all measurement position.

$B_{min}$ : The measured minimum luminance of all measurement position.



















