NHD-3.2-240400EF-CTXI#-CTPBW

TFT (Thin-Film-Transistor) Color Liquid Crystal Display Module

NHD-	Newhaven Display
3.2-	3.2” Diagonal
240400-	240xRGBx400 Pixels
EF-	Model
C-	Built-in Controller
T-	White LED Backlight
X-	TFT
I-	6:00 Optimal View, Wide Temperature
#-	**RoHS Compliant**
CTPBW-	Optically Bonded White Capacitive Touch Panel with Built-in Controller

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Document Revision History

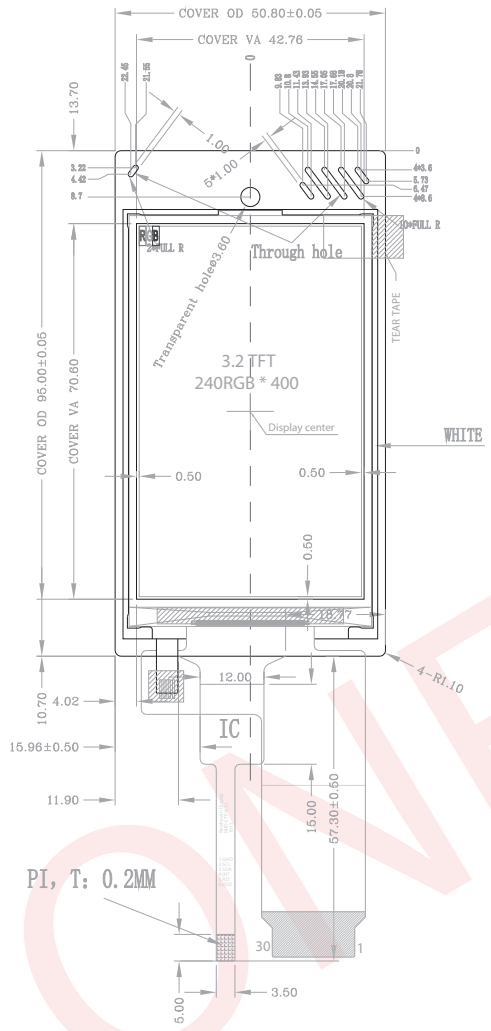
Revision	Date	Description	Changed by
0	3/5/2015	Initial Release	AK
1	3/24/2015	Controller links updated, CTP registers added	AK
2	5/1/2015	CTP mechanical drawing updated	AK
3	1/14/16	Mechanical drawing updated with TFT + CTP bonded view	AK

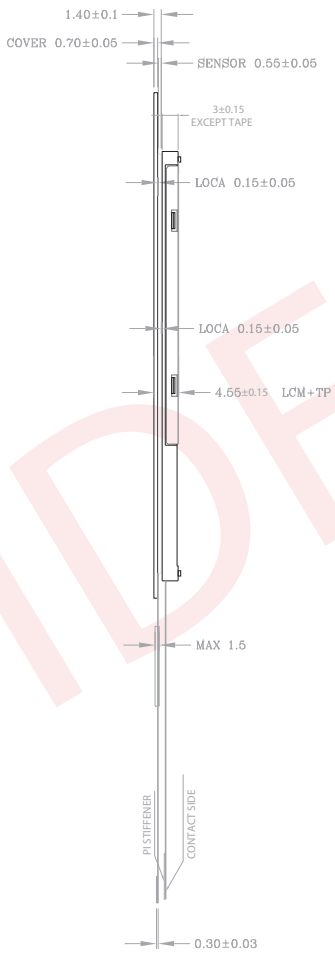
Functions and Features

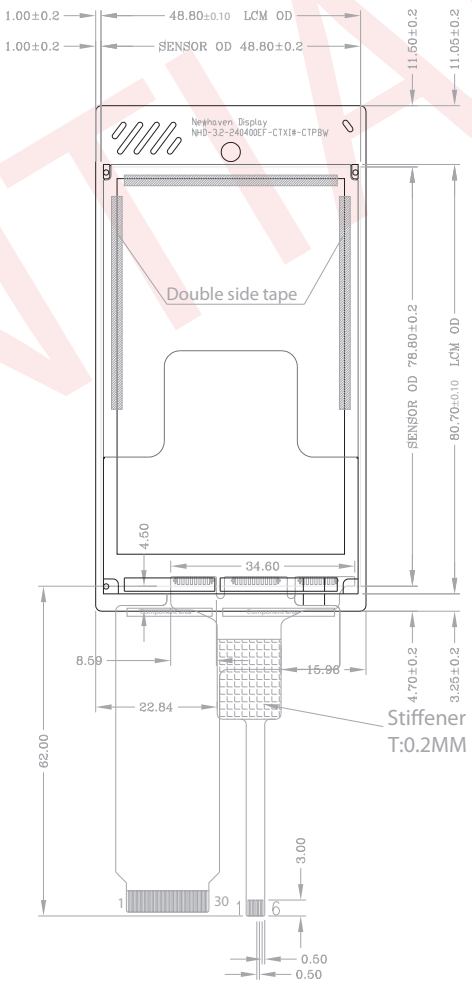
- **240xRGBx400 resolution**
- **LED backlight**
- **18-bit RGB and Serial interface**
- **2.6V~3.3V power supply**
- **Optically bonded Capacitive touch panel with built-in controller**

Mechanical Drawing - TFT + CTP

Rev	Description	Date







	Date	
	01/14/16	NEWHAVEN DISPLAY INTERNATIONAL
Gen. Tolerance ±0.3mm	Unit mm	Model: NHD-3.2-240400EF-CTXI#-CTPBW

Pin Description

TFT Display:

Pin No.	Symbol	External Connection	Function Description
1	GND	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage for LCD and Logic
3	B0	MPU	Blue Data signal
4	B1	MPU	Blue Data signal
5	B2	MPU	Blue Data signal
6	B3	MPU	Blue Data signal
7	B4	MPU	Blue Data signal
8	B5	MPU	Blue Data signal
9	G0	MPU	Green Data signal
10	G1	MPU	Green Data signal
11	G2	MPU	Green Data signal
12	G3	MPU	Green Data signal
13	G4	MPU	Green Data signal
14	G5	MPU	Green Data signal
15	R0	MPU	Red Data signal
16	R1	MPU	Red Data signal
17	R2	MPU	Red Data signal
18	R3	MPU	Red Data signal
19	R4	MPU	Red Data signal
20	R5	MPU	Red Data signal
21	HSYNC	MPU	Horizontal (Line) Sync signal
22	VSYNC	MPU	Vertical (Frame) Sync signal
23	PCLK	MPU	Dot Clock signal
24	DE	MPU	Data Enable signal
25	LED_K	Power Supply	Backlight Cathode
26	LED_A	Power Supply	Backlight Anode
27	SPI_CS	MPU	Active LOW Chip Select signal for Serial Interface. If not used, tie to GND or VDD.
28	SPI_SCL	MPU	Serial Clock signal when SPI_CS = 0. If not used, tie to GND or VDD.
29	SPI_SDI	MPU	Serial Data In signal when SPI_CS = 0. If not used, tie to GND or VDD.
30	SPI_SDO	MPU	Serial Data Out signal when SPI_CS = 0. If not used, tie to GND or VDD.

Recommended LCD connector: 30pin, 0.5mm pitch, FFC connector. Molex P/N: 52892-3095

Capacitive Touch Panel:

Pin No.	Symbol	External Connection	Function Description
1	GND	Power Supply	Ground
2	SCL	MPU	Serial Clock input signal
3	SDA	MPU	Serial Data input signal
4	/INT	MPU	Interrupt signal from touch panel to host
5	/RST	MPU	External interrupt signal from host. 0: Disable /INT; 1: Enable /INT
6	VDD	MPU	Supply Voltage for operation

Electrical Characteristics

TFT:

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	Top	Absolute Max	-20	-	+70	°C
Storage Temperature Range	Tst	Absolute Max	-30	-	+80	°C
Digital Supply Voltage	VDD		2.6	2.8	3.3	V
Supply Current	IDD	VDD=2.8V	-	15	30	mA
"H" Level input	Vih		0.7*VDD	-	VDD	V
"L" Level input	Vil		GND	-	0.3*VDD	V
"H" Level output	Voh		0.8*VDD	-	VDD	V
"L" Level output	Vol		GND	-	0.2*VDD	V
Backlight Supply Voltage	Vled		2.9	3.2	3.5	V
Backlight Supply Current	Iled	Vled=3.2V	-	140	-	mA

Capacitive Touch Panel:

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	Top	Absolute Max	-10	-	+60	°C
Storage Temperature Range	Tst	Absolute Max	-20	-	+70	°C
Supply Voltage	VDD		2.8	3.0	3.3	V
"H" Level input	Vih		0.7*VDD	-	VDD+0.5	V
"L" Level input	Vil		GND-0.5	-	0.3*VDD	V
"H" Level output	Voh		0.8*VDD	-	VDD	V
"L" Level output	Vol		GND	-	0.2*VDD	V

Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing Angle – Top		Cr ≥ 10	-	70	-	°
Viewing Angle – Bottom			-	60	-	°
Viewing Angle – Left			-	70	-	°
Viewing Angle – Right			-	70	-	°
Contrast Ratio	Cr		250	350	-	
Luminance	Lv		340	430	-	cd/m2
Response Time (rise)	Tr		-	20	30	ms
Response Time (fall)	Tf		-	20	30	ms

Viewing angles based on 12:00 grayscale inversion

Controller Information

TFT:

Built-in HX8352-C00(T) controller.
Please download specification at http://www.newhavendisplay.com/app_notes/HX8352-C00T.pdf

Capacitive Touch Panel:

Built-in FT5216 controller.
Please download specification at http://www.newhavendisplay.com/app_notes/FT5x16.pdf
Please download app notes at http://www.newhavendisplay.com/app_notes/FT5x06_registers.pdf

Table of Commands

TFT Display:

Register No.	Register	W/R	Upper Code	Lower Code								Default Value
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R00h	Himax ID	R	-	0	1	1	1	0	0	1	0	0x72
R01h	Display Mode control	W/R	-	DSTB(0)	-	-	-	SCROLL(0)	IDMON(0)	INVON(0)	PTLON(0)	0x00
R02h	Column address start 2	W/R	-	SC[15:8] (8'b0000_0000)								0x00
R03h	Column address start 1	W/R	-	SC[7:0] (8'b0000_0000)								0x00
R04h	Column address end 2	W/R	-	EC[15:8] (8'b0000_0000)								0x00
R05h	Column address end 1	W/R	-	EC[7:0] (8'b1110_1111)								0xEF
R06h	Row address start 2	W/R	-	SP[15:8] (8'b0000_0000)								0x00
R07h	Row address start 1	W/R	-	SP[7:0] (8'b0000_00000)								0x00
R08h	Row address end 2	W/R	-	EP[15:8] (8'b0000_0001)								0x01
R09h	Row address end 1	W/R	-	EP[7:0] (8'b1010_1111)								0xAF
R0Ah	Partial area start row 2	W/R	-	PSL[15:8] (8'b0000_0000)								0x00
R0Bh	Partial area start row 1	W/R	-	PSL[7:0] (8'b0000_00000)								0x00
R0Ch	Partial area end row 2	W/R	-	PEL[15:8] (8'b0000_0001)								0x01
R0Dh	Partial area end row 1	W/R	-	PEL[7:0] (8'b1010_1111)								0xAF
R0Eh	Vertical Scroll Top fixed area 2	W/R	-	TFA[15:8] (8'b0000_0000)								0x00
R0Fh	Vertical Scroll Top fixed area 1	W/R	-	TFA[7:0] (8'b0000_0000)								0x00
R10h	Vertical Scroll height area 2	W/R	-	VSA[15:8] (8'b0000_0001)								0x01
R11h	Vertical Scroll height area 1	W/R	-	VSA[7:0] (8'b1011_0000)								0xB0
R12h	Vertical Scroll Button area 2	W/R	-	BFA[15:8] (8'b0000_0000)								0x00
R13h	Vertical Scroll Button area 1	W/R	-	BFA [7:0] (8'b0000_0000)								0x00
R14h	Vertical Scroll Start address 2	W/R	-	VSP [15:8] (8'b0000_0000)								0x00
R15h	Vertical Scroll Start address 1	W/R	-	VSP [7:0] (8'b0000_0000)								0X00
R16h	Memory Access control	W/R	-	MY(0)	MX(0)	MV(0)	ML(0)	BGR(0)	-	-	-	0x00
R17h	COLMOD	W/R	-	-	CSEL[2:0] (3b'110)			-	IFPF[2:0] (3b'110)			0x66
R18h	OSC Control 2	W/R	-	-	-	-	-	RADJ[2:0](4b'0100)				0x04
R19h	OSC Control 1	W/R	-	-	-	-	-	-	-	-	OSC_EN(0)	0x00
R1Ah	Power Control 1	W/R	-	-	-	-	-	-	BT[2:0] (100)			0x04
R1Bh	Power Control 2	W/R	-	VCIRE(1)	-	-	VRH[4:0] (0_1100)					0x8C
R1Ch	Power Control 3	W/R	-	-	-	-	-	-	AP[2:0] (011)			0x03
R1Fh	Power Control 5	W/R	-	GASEN(1)	VCOMG(0)	-	PON(0)	DK(1)	XDK(0)	DDVDH_TRI(0)	STB(1)	0x89
R22h	SRAM Write Control	W/R	SRAM Write									-
R23h	VCOM Control 1	W/R	-	-	-	-	-	-	-	-	SELVCM(0)	0x00
R24h	VCOM Control 2	W/R	-	-	VCM[6:0](100_0000)							0x40
R25h	VCOM Control 3	W/R	-	-	-	-	VDV[4:0](0_1111)					0x0F
R26h	Display Control 1	W/R	-	-	-	-	PTG(0)	ISC[3:0](0001)				0x01

Register No.	Register	W/R	Upper Code	Lower Code								Default Value
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R27h	Display Control 2	W/R	-	-	-	-	-	-	-	-	REF(1)	0x01
R28h	Display Control 3	W/R	-	-	-	GON(1)	DTE(0)	D[1:0] (00)		-	-	0x30
R29h	Display Control 4	W/R	-	-	-	NL[5:0](6'b11_0101)						0x35
R2Ah	Display Control 5	W/R	-	-	SCN[6:0](000_0000)							0x00
R2Bh	Display Control 6	W/R	-	-	-	-	-	-	-	PTS[1:0](00)		0x00
R2Ch	Display Control 7	W/R	-	-	-	-	-	-	-	DIVE[1:0](10)		0x02
R2Dh	Cycle Control 1	W/R	-	-	SDT[2:0](000)			-	NOW[2:0](110)			0x06
R2Eh	Cycle Control 2	W/R	-	NW[5:0](00_0000)								0x00
R31h	RGB interface control 1	W/R	-	-	-	-	RM(0)	-	-	DM[1:0](00)		0x00
R32h	RGB interface control 2	W/R	-	SDA_EN(0)	-	-	VSPL (0)	HSPL (0)	-	EPL(1)	DPL(0)	0x02
R33h	RGB interface control 3	W/R	-	HBP[7:0](8'b0000_1000)								0x08
R34h	RGB interface control 4	W/R	-	HBP[9:8](2'b00)		VBP[5:0](6'b00_0100)						0x04
R36h	Panel Characteristic	W/R	-	-	-	-	REV_PANEL (0)	SM_PANEL (0)	GS_PANEL(0)l	BGR_PANEL(0)	SS_PANEL (0)	0x00
R38h	OTP Control 1	W/R	-	OTP_MASK[7:0] (8'h00)								0x00
R39h	OTP Control 2	W/R	-	OTP_INDEX[7:0] (8'h00)								0x00
R3Ah	OTP Control 3	W/R	-	-	VPP_EN (0)	OTP_POR(0)	OTP_PWE(0)	OTP_PTM[1:0] (00)		VPP_SEL (0)	OTP_PROG(0)	0x00
R3Bh	OTP Control 4	R	-	OTP_DATA[7:0]								0xFF
R3Ch	CABC Control 1	W/R	-	DBV[7:0] (8'h00)								0x00
R3Dh	CABC Control 2	W/R	-	-	-	BCTRL (0)	-	DD(0)	BL(0)	-	-	0x00
R3Eh	CABC Control 3	W/R	-	-	-	-	-	-	-	CACB[1:0] (00)		0x00
R3Fh	CABC Control 4	W/R	-	CMB[7:0] (8'h00)								0x00
R40h	Gamma Control 1	W/R	-	-	KP1[2:0](100)			-	KP0[2:0](100)			0x44
R41h	Gamma Control 2	W/R	-	-	KP3[2:0](100)			-	KP2[2:0](100)			0x44
R42h	Gamma Control 3	W/R	-	-	KP5[2:0](100)			-	KP4[2:0](100)			0x44
R43h	Gamma Control 4	W/R	-	-	RP1[2:0](100)			-	RP0[2:0](100)			0x44
R44h	Gamma Control 5	W/R	-	-	-	-	-	VRP0[3:0]				0x08
R45h	Gamma Control 6	W/R	-	-	-	-	VRP1[4:0]					0x10
R46h	Gamma Control 7	W/R	-	-	KN1[2:0](100)			-	KN0[2:0](100)			0x44
R47h	Gamma Control 8	W/R	-	-	KN3[2:0](100)			-	KN2[2:0](100)			0x44
R48h	Gamma Control 9	W/R	-	-	KN5[2:0](100)			-	KN4[2:0](100)			0x44
R49h	Gamma Control 10	W/R	-	-	RN1[2:0](100)			-	RN0[2:0](100)			0x44
R4Ah	Gamma Control 11	W/R	-	-	-	-	-	0x08				0x08
R4Bh	Gamma Control 12	W/R	-	-	-	-	VRN1[3:0]					0x10
R4Ch	Gamma Control 13	W/R	-	VREP1[3:0]				VREP0[3:0]				0x88
R4Dh	Gamma Control 14	W/R	-	VREN0[3:0]				VREP2[3:0]				0x88
R4Eh	Gamma Control 15	W/R	-	VREN2[3:0]				VREN1[3:0]				0x88
R60h	TE Control	W/R	-	-	-		TE_MODE(0)	TEON (0)		-	-	0x00
R61h	ID1	W/R	-	ID1[7:0](8'h00)								0x00
R62h	ID2	W/R	-	ID2[7:0](8'h00)								0x00
R63h	ID3	W/R	-	ID3[7:0](8'h00)								0x00
R68h	Memory Write Control	W/R	-	-	-	-	-	-	-	WEMODE (1)	-	0x02
R69h	TE Interval Control	W/R	-	-	-	-	-	-	TEI[2:0](000)			0x00
R6Ah	RGB SRAM Cycle	W/R	-	-	-	-	-	-	DENC[2:0](000)			0x00
R6Bh	Data Format Control	W/R	-	-	-	EPF[1:0](10)		-	-	-	DFM(0)	0x20
R70h	Frame Rate Control 1	W/R	-	-	-	-	BC0(1)	-	-	DIV0[1:0](00)		0x10
R71h	Frame Rate Control 2	W/R	-	-	-	-	RTN0[4:0](1_0000)					0x10
R72h	Frame Rate Control 3	W/R	-	BP0[7:0](8'h02)								0x02
R73h	Frame Rate Control 4	W/R	-	FP0[7:0](8'h02)								0x02
R74h	Frame Rate Control 5	W/R	-	-	-	-	BC2(0)	-	-	DIV2[1:0](00)		0x00
R75h	Frame Rate Control 6	W/R	-	-	-	-	RTN2[4:0](1_0000)					0x10

Register No.	Register	W/R	Upper Code	Lower Code								Default Value
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R76h	Frame Rate Control 7	W/R	-	BP2[7:0](8'h02)								0x02
R77h	Frame Rate Control 8	W/R	-	FP2[7:0](8'h02)								0x02
R7Ah	Power Control 6	W/R	-	-	-	-	-	-	SAP0[2:0](001)			0x01
R7Bh	Power Control 7	W/R	-	-	DC10[2:0](100)			-	DC00[2:0](100)			0x44
R7Ch	Power Control 8	W/R	-	-	-	-	-	-	SAP1[2:0](001)			0x01
R7Dh	Power Control 9	W/R	-	-	DC11[2:0](100)			-	DC01[2:0](100)			0x44
R7Eh	Power Control 10	W/R	-	-	-	-	-	-	SAP2[2:0](001)			0x01
R7Fh	Power Control 11	W/R	-	-	DC12[2:0](100)			-	DC02[2:0](100)			0x44
R84h	TE Output Line 2	W/R	-	TSEL[15:8](8'h00)								0x00
R85h	TE Output Line 1	W/R	-	TSEL[7:0](8'h00)								0x00
R86h	VPP Control	W/R	-	-	-	-	-	-	VPP[2:0](011)			0x03
R87h	OTP Control 5	W/R	-	OTP_KEY[7:0](8'h55)								0x55
R88h	Get Scan Line 2	R	-	SL[15:8](8'hFF)								0xFF
R89h	Get Scan Line 1	R	-	SL[7:0](8'hFF)								0xFF
R8Ah	Read VCOM OTP Times	R	-	-	-	-	-	VCOM_OTP_TIMES[3:0]				0x00
R8Bh	Read ID OTP Times	R	-	-	-	-	-	ID_OTP_TIMES[3:0]				0x00
RFFh	Page select	W/R	-	-	-	-	-	-	-	PAGE_SEL[1:0] (00)		0x00

Register No.	Register	W/R	Upper Code	Lower Code								Default Value
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R00h	DGC Control	W/R	-	-	-	-	-	-	-	-	DGC_EN(0)	0x00
R01h	DGC LUT1	W	-	DGC_LUT_R00(8'h00)								0x00
R02h	DGC LUT2	W	-	DGC_LUT_R01(8'h08)								0x08
R03h	DGC LUT3	W	-	DGC_LUT_R02(8'h10)								0x10
R04h	DGC LUT4	W	-	DGC_LUT_R03(8'h18)								0x18
R05h	DGC LUT5	W	-	DGC_LUT_R04(8'h20)								0x20
R06h	DGC LUT6	W	-	DGC_LUT_R05(8'h28)								0x28
R07h	DGC LUT7	W	-	DGC_LUT_R06(8'h30)								0x30
R08h	DGC LUT8	W	-	DGC_LUT_R07(8'h38)								0x38
R09h	DGC LUT9	W	-	DGC_LUT_R08(8'h40)								0x40
R0Ah	DGC LUT10	W	-	DGC_LUT_R09(8'h48)								0x48
R0Bh	DGC LUT11	W	-	DGC_LUT_R10(8'h50)								0x50
R0Ch	DGC LUT12	W	-	DGC_LUT_R11(8'h58)								0x58
R0Dh	DGC LUT13	W	-	DGC_LUT_R12(8'h60)								0x60
R0Eh	DGC LUT14	W	-	DGC_LUT_R13(8'h68)								0x68
R0Fh	DGC LUT15	W	-	DGC_LUT_R14(8'h70)								0x70
R10h	DGC LUT16	W	-	DGC_LUT_R15(8'h78)								0x78
R11h	DGC LUT17	W	-	DGC_LUT_R16(8'h80)								0x80
R12h	DGC LUT18	W	-	DGC_LUT_R17(8'h88)								0x88
R13h	DGC LUT19	W	-	DGC_LUT_R18(8'h90)								0x90
R14h	DGC LUT20	W	-	DGC_LUT_R19(8'h98)								0x98
R15h	DGC LUT21	W	-	DGC_LUT_R20(8'hA0)								0xA0
R16h	DGC LUT22	W	-	DGC_LUT_R21(8'hA8)								0xA8
R17h	DGC LUT23	W	-	DGC_LUT_R22(8'hB0)								0xB0
R18h	DGC LUT24	W	-	DGC_LUT_R23(8'hB8)								0xB8
R19h	DGC LUT25	W	-	DGC_LUT_R24(8'hC0)								0xC0
R1Ah	DGC LUT26	W	-	DGC_LUT_R25(8'hC8)								0xC8
R1Bh	DGC LUT27	W	-	DGC_LUT_R26(8'hD0)								0xD0
R1Ch	DGC LUT28	W	-	DGC_LUT_R27(8'hD8)								0xD8
R1Dh	DGC LUT29	W	-	DGC_LUT_R28(8'hE0)								0xE0
R1Eh	DGC LUT30	W	-	DGC_LUT_R29(8'hE8)								0xE8
R1Fh	DGC LUT31	W	-	DGC_LUT_R30(8'hF0)								0xF0
R20h	DGC LUT32	W	-	DGC_LUT_R31(8'hF8)								0xF8
R21h	DGC LUT33	W	-	DGC_LUT_R32(8'hFC)								0xFC
R22h	DGC LUT34	W	-	DGC_LUT_G00(8'h00)								0x00
R23h	DGC LUT35	W	-	DGC_LUT_G01(8'h08)								0x08
R24h	DGC LUT36	W	-	DGC_LUT_G02(8'h10)								0x10
R25h	DGC LUT37	W	-	DGC_LUT_G03(8'h18)								0x18
R26h	DGC LUT38	W	-	DGC_LUT_G04(8'h20)								0x20
R27h	DGC LUT39	W	-	DGC_LUT_G05(8'h28)								0x28
R28h	DGC LUT40	W	-	DGC_LUT_G06(8'h30)								0x30
R29h	DGC LUT41	W	-	DGC_LUT_G07(8'h38)								0x38
R2Ah	DGC LUT42	W	-	DGC_LUT_G08(8'h40)								0x40
R2Bh	DGC LUT43	W	-	DGC_LUT_G09(8'h48)								0x48
R2Ch	DGC LUT44	W	-	DGC_LUT_G10(8'h50)								0x50
R2Dh	DGC LUT45	W	-	DGC_LUT_G11(8'h58)								0x58
R2Eh	DGC LUT46	W	-	DGC_LUT_G12(8'h60)								0x60
R2Fh	DGC LUT47	W	-	DGC_LUT_G13(8'h68)								0x68
R30h	DGC LUT48	W	-	DGC_LUT_G14(8'h70)								0x70
R31h	DGC LUT49	W	-	DGC_LUT_G15(8'h78)								0x78
R32h	DGC LUT50	W	-	DGC_LUT_G16(8'h80)								0x80
R33h	DGC LUT51	W	-	DGC_LUT_G17(8'h88)								0x88
R34h	DGC LUT52	W	-	DGC_LUT_G18(8'h90)								0x90
R35h	DGC LUT53	W	-	DGC_LUT_G19(8'h98)								0x98
R36h	DGC LUT54	W	-	DGC_LUT_G20(8'hA0)								0xA0
R37h	DGC LUT55	W	-	DGC_LUT_G21(8'hA8)								0xA8
R38h	DGC LUT56	W	-	DGC_LUT_G22(8'hB0)								0xB0
R39h	DGC LUT57	W	-	DGC_LUT_G23(8'hB8)								0xB8
R3Ah	DGC LUT58	W	-	DGC_LUT_G24(8'hC0)								0xC0
R3Bh	DGC LUT59	W	-	DGC_LUT_G25(8'hC8)								0xC8
R3Ch	DGC LUT60	W	-	DGC_LUT_G26(8'hD0)								0xD0
R3Dh	DGC LUT61	W	-	DGC_LUT_G27(8'hD8)								0xD8
R3Eh	DGC LUT62	W	-	DGC_LUT_G28(8'hE0)								0xE0
R3Fh	DGC LUT63	W	-	DGC_LUT_G29(8'hE8)								0xE8
R40h	DGC LUT64	W	-	DGC_LUT_G30(8'hF0)								0xF0
R41h	DGC LUT65	W	-	DGC_LUT_G31(8'hF8)								0xF8
R42h	DGC LUT66	W	-	DGC_LUT_G32(8'hFC)								0xFC

Register No.	Register	W/R	Upper Code	Lower Code								Default Value
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R43h	DGC LUT67	W	-	DGC_LUT_B00(8'h00)								0x00
R44h	DGC LUT68	W	-	DGC_LUT_B01(8'h08)								0x08
R45h	DGC LUT69	W	-	DGC_LUT_B02(8'h10)								0x10
R46h	DGC LUT70	W	-	DGC_LUT_B03(8'h18)								0x18
R47h	DGC LUT71	W	-	DGC_LUT_B04(8'h20)								0x20
R48h	DGC LUT72	W	-	DGC_LUT_B05(8'h28)								0x28
R49h	DGC LUT73	W	-	DGC_LUT_B06(8'h30)								0x30
R4Ah	DGC LUT74	W	-	DGC_LUT_B07(8'h38)								0x38
R4Bh	DGC LUT75	W	-	DGC_LUT_B08(8'h40)								0x40
R4Ch	DGC LUT76	W	-	DGC_LUT_B09(8'h48)								0x48
R4Dh	DGC LUT77	W	-	DGC_LUT_B10(8'h50)								0x50
R4Eh	DGC LUT78	W	-	DGC_LUT_B11(8'h58)								0x58
R4Fh	DGC LUT79	W	-	DGC_LUT_B12(8'h60)								0x60
R50h	DGC LUT80	W	-	DGC_LUT_B13(8'h68)								0x68
R51h	DGC LUT81	W	-	DGC_LUT_B14(8'h70)								0x70
R52h	DGC LUT82	W	-	DGC_LUT_B15(8'h78)								0x78
R53h	DGC LUT83	W	-	DGC_LUT_B16(8'h80)								0x80
R54h	DGC LUT84	W	-	DGC_LUT_B17(8'h88)								0x88
R55h	DGC LUT85	W	-	DGC_LUT_B18(8'h90)								0x90
R56h	DGC LUT86	W	-	DGC_LUT_B19(8'h98)								0x98
R57h	DGC LUT87	W	-	DGC_LUT_B20(8'hA0)								0xA0
R58h	DGC LUT88	W	-	DGC_LUT_B21(8'hA8)								0xA8
R59h	DGC LUT89	W	-	DGC_LUT_B22(8'hB0)								0xB0
R5Ah	DGC LUT90	W	-	DGC_LUT_B23(8'hB8)								0xB8
R5Bh	DGC LUT91	W	-	DGC_LUT_B24(8'hC0)								0xC0
R5Ch	DGC LUT92	W	-	DGC_LUT_B25(8'hC8)								0xC8
R5Dh	DGC LUT93	W	-	DGC_LUT_B26(8'hD0)								0xD0
R5Eh	DGC LUT94	W	-	DGC_LUT_B27(8'hD8)								0xD8
R5Fh	DGC LUT95	W	-	DGC_LUT_B28(8'hE0)								0xE0
R60h	DGC LUT96	W	-	DGC_LUT_B29(8'hE8)								0xE8
R61h	DGC LUT97	W	-	DGC_LUT_B30(8'hF0)								0xF0
R62h	DGC LUT98	W	-	DGC_LUT_B31(8'hF8)								0xF8
R63h	DGC LUT99	W	-	DGC_LUT_B32(8'hFC)								0xFC
RC3h	CABC Control 5	W/R	-	LEDONPOL (0)	PWMDIV[2:0](000)			SEL_GAIN[1:0] (11)		INVPLUS(1)	SEL_BLDUTY (1)	0x0F
RC5h	CABC Control 7	W/R	-	PWM_PERIOD[7:0](8'h23)								0x23
RFFh	Page select	W/R	-	-	-	-	-	-	-	PAGE_SEL[1:0](00)		0x00

For detailed command descriptions, please download specification at
http://www.newhavendisplay.com/app_notes/HX8352-C00T.pdf

Capacitive Touch Panel:

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0	Access
00h	DEVICE_MODE		Device Mode [2..0]							R/W
01h	GEST_ID	Gesture ID [7..0]								R
02h	TD_STATUS						Touch Points [3..0]			R
03h	TOUCH1_XH	Event Flag				1st Touch X Position MSB [11..8]				R
04h	TOUCH1_XL	1st Touch X Position LSB [7..0]								R
05h	TOUCH1_YH	Touch ID [3..0]				1st Touch Y Position MSB [11..8]				R
06h	TOUCH1_YL	1st Touch Y Position LSB [7..0]								R
07h										R
08h										R
09h	TOUCH2_XH	Event Flag				2nd Touch X Position MSB [11..8]				R
0Ah	TOUCH2_XL	2nd Touch X Position LSB [7..0]								R
0Bh	TOUCH2_YH	Touch ID [3..0]				2nd Touch Y Position MSB [11..8]				R
0Ch	TOUCH2_YL	2nd Touch Y Position LSB [7..0]								R
0Dh										R
0Eh										R
0Fh	TOUCH3_XH	Event Flag				3rd Touch X Position MSB [11..8]				R
10h	TOUCH3_XL	3rd Touch X Position LSB [7..0]								R
11h	TOUCH3_YH	Touch ID [3..0]				3rd Touch Y Position MSB [11..8]				R
12h	TOUCH3_YL	3rd Touch Y Position LSB [7..0]								R
13h										R
14h										R
15h	TOUCH4_XH	Event Flag				4th Touch X Position MSB [11..8]				R
16h	TOUCH4_XL	4th Touch X Position LSB [7..0]								R
17h	TOUCH4_YH	Touch ID [3..0]				4th Touch Y Position MSB [11..8]				R
18h	TOUCH4_YL	4th Touch Y Position LSB [7..0]								R
19h										R
1Ah										R
1Bh	TOUCH5_XH	Event Flag				5th Touch X Position MSB [11..8]				R
1Ch	TOUCH5_XL	5th Touch X Position LSB [7..0]								R
1Dh	TOUCH5_YH	Touch ID [3..0]				5th Touch Y Position MSB [11..8]				R
1Eh	TOUCH5_YL	5th Touch Y Position LSB [7..0]								R
1Fh										R

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0	Access
80h	ID_G_THGROUP	valid touching detect threshold								R/W
81h	ID_G_THPEAK	valid touching peak detect threshold								R/W
82h	ID_G_THCAL	the threshold when calculating the focus of touching								R/W
83h	ID_G_THWATER	the threshold when there is surface water								R/W
84h	ID_G_TEMP	the threshold of temperature compensation								R/W
85h	ID_G_THDIFF	the threshold whether the coordinate is different from original								R/W
86h	ID_G_CTRL					Power Control Mode [1..0]				R/W
87h	ID_G_TIME_ENTER_MONITOR	the timer for entering monitor status								R/W
88h	ID_G_PERIODACTIVE					Period Active [3..0]				R/W
89h	ID_G_PERIODMONITOR	the timer of entering idle when in monitor status								R/W
A0h	ID_G_AUTO_CLB_MODE	auto calibration mode								R/W
A1h	ID_G_LIB_VERSION_H	Firmware Library Version H byte								R
A2h	ID_G_LIB_VERSION_L	Firmware Library Version L byte								R
A3h	ID_G_CIPHER	Chip vendor ID								R
A4h	ID_G_MODE	the interrupt status to host								R
A5h	ID_G_PMODE	Power Consume Mode								
A6h	ID_G_FIRMID	Firmware ID								R
A7h	ID_G_STATE	Running State								
A8h	ID_G_FT5201ID	CTPM Vendor ID								R
A9h	ID_G_ERR	Error Code								R
AAh	ID_G_CLB	Configure TP module during calibration in Test Mode								R/W
FEh	LOG_MSG_CNT	The log MSG count								R
FFh	LOG_CUR_CHA	Current character of log message								R

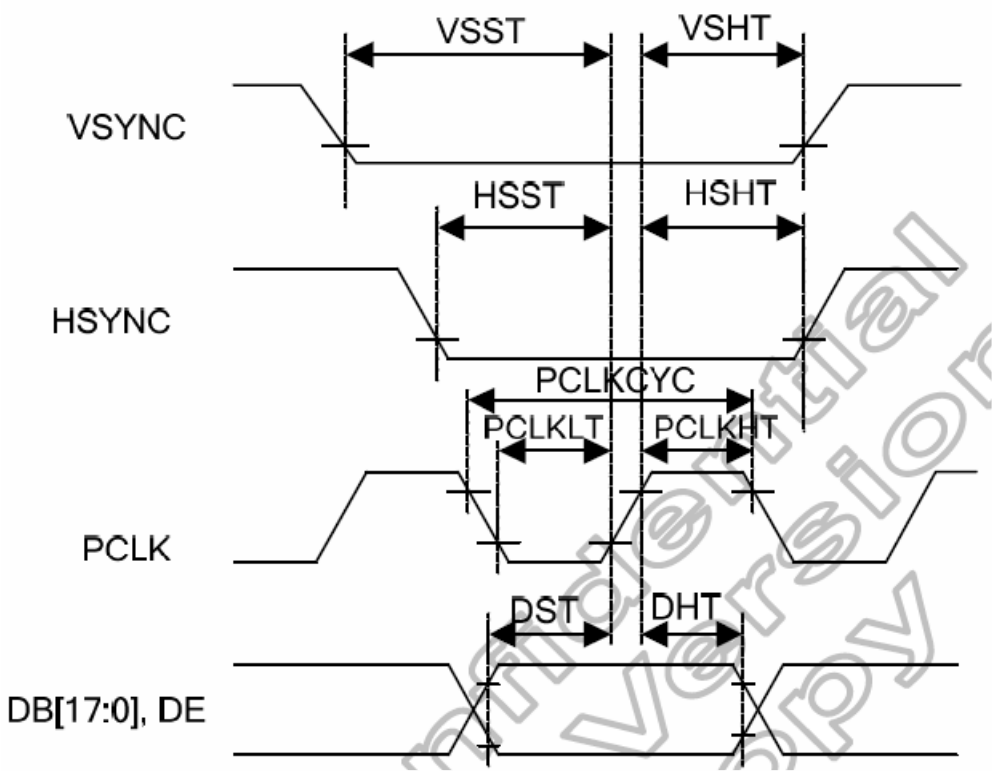
NOTE: Registers 80h – AFh have been configured for optimum settings and do not need to be modified.

Register No	Register Name	Bits	Value	Description
00h	Device Mode	[2:0]	000b	Normal Operating Mode
			100b	Test Mode - read raw data (reserved)
			001b	System Information Mode (reserved)
01h	Gesture ID	[7:0]	48h	Zoom In
			49h	Zoom Out
			00h	No Gesture
02h	Touch Points	[3:0]	000b	0 touch points detected
			001b	1 touch point detected
			010b	2 touch points detected
			011b	3 touch points detected
			100b	4 touch points detected
			101b	5 touch points detected
03h	Touch 1 Event Flag	[7:6]	00b	Put Down
			01b	Put Up
			10b	Contact
			11b	Reserved
03h	TOUCH1_XH	[3:0]	0h - 1h	Upper 4 bits of X touch coordinate
04h	TOUCH1_XL	[7:0]	00h - FFh	Lower 8 bits of X touch coordinate
05h	TOUCH1_YH	[3:0]	0h - 1h	Upper 4 bits of Y touch coordinate
06h	TOUCH1_YL	[7:0]	00h - FFh	Lower 8 bits of Y touch coordinate
09h	Touch 2 Event Flag	[7:6]	00b	Put Down
			01b	Put Up
			10b	Contact
			11b	Reserved
09h	TOUCH2_XH	[3:0]	0h - 1h	Upper 4 bits of X touch coordinate
0Ah	TOUCH2_XL	[7:0]	00h - FFh	Lower 8 bits of X touch coordinate
0Bh	TOUCH2_YH	[3:0]	0h - 1h	Upper 4 bits of Y touch coordinate
0Ch	TOUCH2_YL	[7:0]	00h - FFh	Lower 8 bits of Y touch coordinate
0Fh	Touch 3 Event Flag	[7:6]	00b	Put Down
			01b	Put Up
			10b	Contact
			11b	Reserved
0Fh	TOUCH3_XH	[3:0]	0h - 1h	Upper 4 bits of X touch coordinate
10h	TOUCH3_XL	[7:0]	00h - FFh	Lower 8 bits of X touch coordinate
11h	TOUCH3_YH	[3:0]	0h - 1h	Upper 4 bits of Y touch coordinate
12h	TOUCH3_YL	[7:0]	00h - FFh	Lower 8 bits of Y touch coordinate
15h	Touch 4 Event Flag	[7:6]	00b	Put Down
			01b	Put Up
			10b	Contact
			11b	Reserved
15h	TOUCH4_XH	[3:0]	0h - 1h	Upper 4 bits of X touch coordinate
16h	TOUCH4_XL	[7:0]	00h - FFh	Lower 8 bits of X touch coordinate
17h	TOUCH4_YH	[3:0]	0h - 1h	Upper 4 bits of Y touch coordinate
18h	TOUCH4_YL	[7:0]	00h - FFh	Lower 8 bits of Y touch coordinate

Register No	Register Name	Bits	Value	Description
1Bh	Touch 5 Event Flag	[7:6]	00b	Put Down
			01b	Put Up
			10b	Contact
			11b	Reserved
1Bh	TOUCH5_XH	[3:0]	0h - 1h	Upper 4 bits of X touch coordinate
1Ch	TOUCH5_XL	[7:0]	00h - FFh	Lower 8 bits of X touch coordinate
1Dh	TOUCH5_YH	[3:0]	0h - 1h	Upper 4 bits of Y touch coordinate
1Eh	TOUCH5_YL	[7:0]	00h - FFh	Lower 8 bits of Y touch coordinate
80h	ID_G_THGROUP	[7:0]	00h - FFh	Valid touching detect threshold Recommended: 46h
				Actual value will be 4 times register's value
81h	ID_G_THPEAK	[7:0]	00h - FFh	valid touching peak detect threshold Recommended: 3Ch
82h	ID_G_THCAL	[7:0]	00h - FFh	Touch focus threshold Recommended: 1Dh
83h	ID_G_THWATER	[7:0]	00h - FFh	threshold when there is surface water Recommended: D3h
84h	ID_G_THTEMP	[7:0]	00h- FFh	threshold of temperature compensation Recommended: EBh
85h	ID_G_THDIFF	[7:0]	00h- FFh	Touch difference threshold Recommended: A0h
				Actual value is 32 times the register's value
86h	ID_G_CTRL	[1:0]	00h	Power Control Mode: Not Auto Jump
			01h	Power Control Mode: Auto Jump
87h	ID_G_TIME_ENTER_MONITOR	[7:0]	00h-FFh	Delay to enter 'Monitor' status (s) Recommended: C8h
88h	ID_G_PERIODACTIVE	[3:0]	3h-Eh	Period of 'Active' status (ms) Recommended: 6h
89h	ID_G_PERIODMONITOR	[7:0]	1Eh-FFh	Timer to enter 'idle' when in 'Monitor' (ms) Recommended: 28h
A0h	ID_G_AUTO_CLB_MODE	[7:0]	00h	Auto calibration mode: Enable auto calibration
			FFh	Auto calibration mode: Disable auto calibration
A1h	ID_G_LIB_VERSION_H	[7:0]	30h	Firmware Library Version H byte
A2h	ID_G_LIB_VERSION_L	[7:0]	01h	Firmware Library Version L byte
A3h	ID_G_CIPHER	[7:0]	06h	Chip vendor ID
A4h	ID_G_MODE	[0:0]	00h	Interrupt status: Enable interrupt to host
			01h	Interrupt status: Disable interrupt to host
A5h	ID_G_PMODE	[1:0]	00h	'Active' Mode
			01h	'Monitor' Mode
			03h	'Hibernate' Mode
A6h	ID_G_FIRMID	[7:0]	30h	Firmware ID
A7h	ID_G_STATE	[7:0]	00h	Running State: Configure
			01h	Running State: Work
			02h	Running State: Calibration
			03h	Running State: Factory
			04h	Running State: Auto-calibration
A8h	ID_G_FT5201ID	[7:0]	98h	CTPM Vendor's Chip ID
A9h	ID_G_ERR	[7:0]	00h	Error Code: OK
			03h	Error Code: Chip register writing inconsistent with reading
			05h	Error Code: Chip start fail
			1Ah	Error Code: Calibration match fail

Timing Characteristics

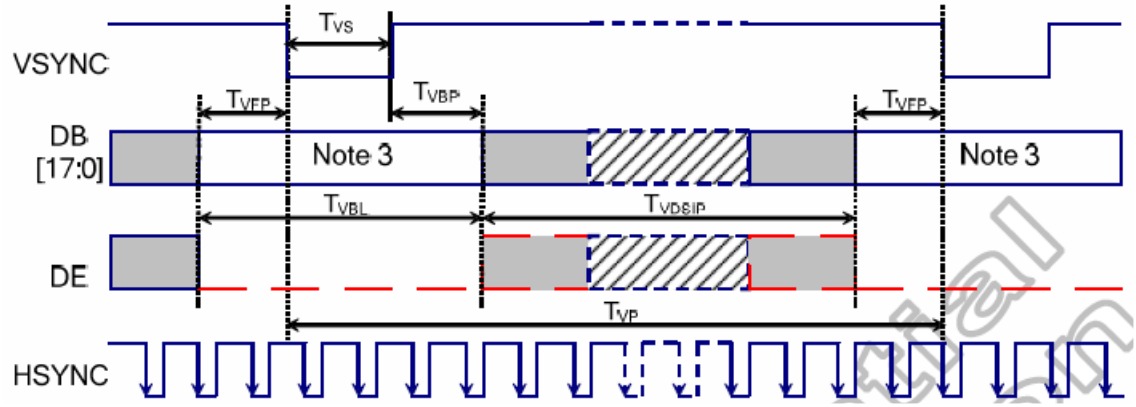
RGB Interface:



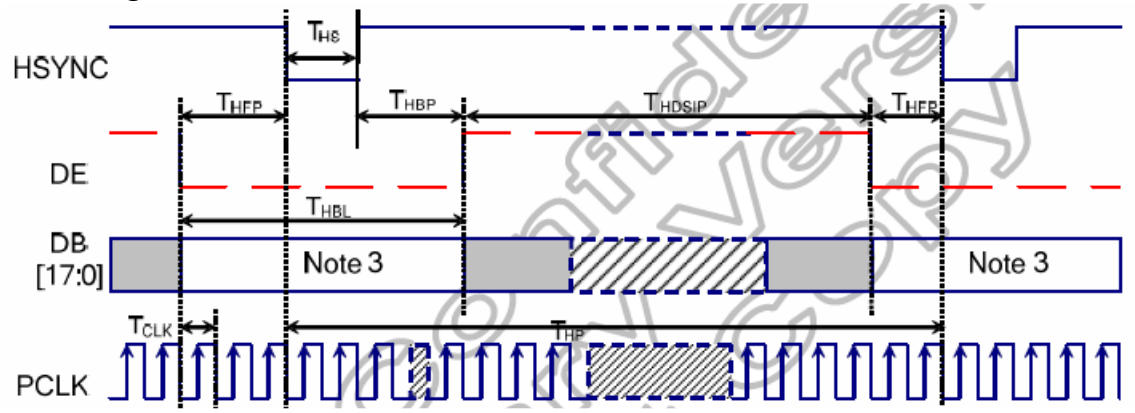
Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Vertical sync. Setup Time	VSST	-	10	-	-	ns
Vertical sync. Hold Time	VSHT	-	10	-	-	ns
Horizontal sync. Setup Time	HSST	-	10	-	-	ns
Horizontal sync. Hold Time	HSHT	-	10	-	-	ns
Pixel Clock Cycle	PCLKCYC	18-/ 16-bit	100	-	-	ns
Pixel Clock Setup Time	PLCKLT	-	10	-	-	ns
Pixel Clock High Time	PCLKHT	-	10	-	-	ns
Data Setup Time DB[17:0], Enable	DST	-	10	-	-	ns
Data Hold Time DB[17:0], Enable	DHT	-	10	-	-	ns

Note: (1) Signal rise and fall times are equal or less than 20ns.
(2) Measure of input signals are using 0.3xIOVCC for low state and 0.7xIOVCC for high state.

Vertical Timing for RGB Interface:



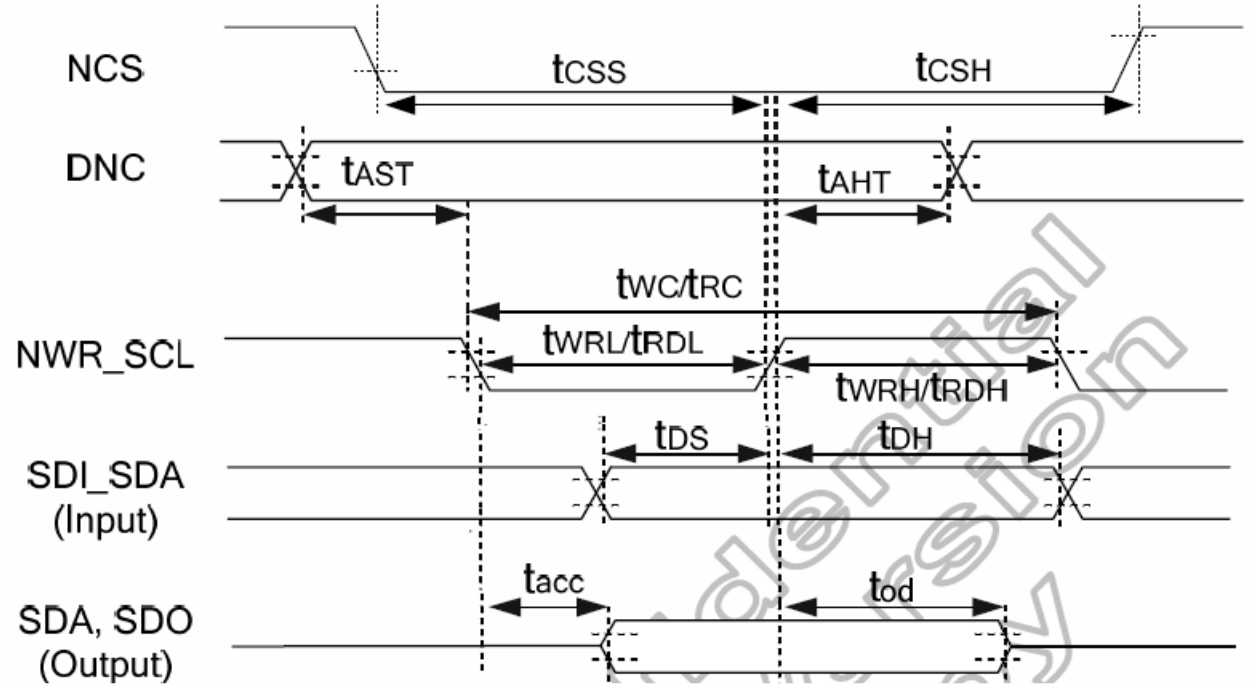
Horizontal Timing for RGB Interface:



Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}	-	438	-	503	HS
Vertical low pulse width	T_{VS}	-	2	2	-	HS
Vertical front porch	T_{VFP}	-	2	2	6	HS
Vertical back porch	T_{VBP}	-	2	6	63	HS
Vertical blanking period	T_{VBL}	$T_{VS} + T_{VBP} + T_{VFP}$	6	10	71	HS
Vertical active area	T_{VDISP}	-	-	432	-	HS
			-		-	HS
					-	HS
Vertical refresh rate	T_{VRR}	Frame rate	50	60	80	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	-	246	-	1008	PCLK
Horizontal low pulse width	T_{HS}	-	2	2	256	PCLK
Horizontal front porch	T_{HFP}	-	2	2	256	PCLK
Horizontal back porch	T_{HBP}	-	2	6	256	PCLK
Horizontal blanking period	T_{HBL}	$T_{HS} + T_{HBP} + T_{HFP}$	6	10	768	PCLK
Horizontal active area	T_{HDISP}	-	-	240	-	PCLK
Pixel clock cycle	f_{CLKCYC}	-	5.39	-	16.6	MHz

Note: (1) IOVCC=1.65 to 3.3V, VCI=2.5 to 3.3V, VSSA=VSSD=0V, Ta=-30 to 70℃ (to +85℃ no damage)
(2) Data lines can be set to "High" or "Low" during blanking time – Don't care.
(3) HP is multiples of PCLK.

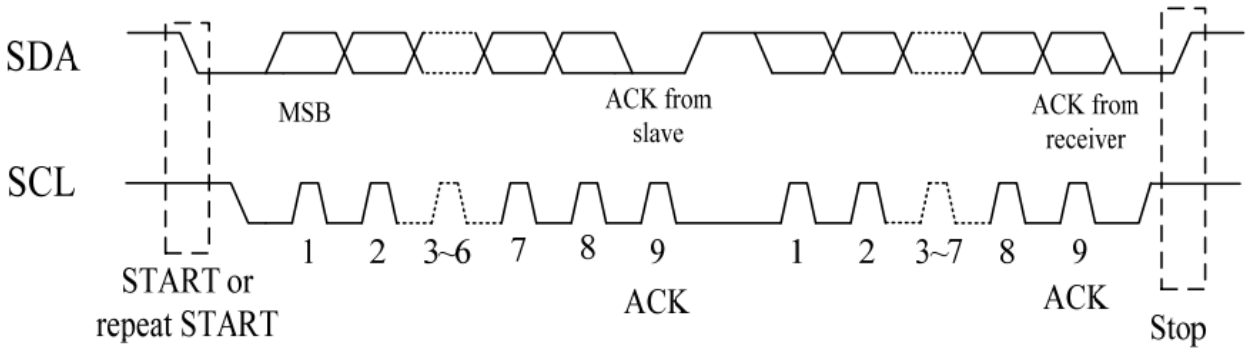
Serial Interface:



Signal	Symbol	Parameter	Min.	Max.	Unit	Description
NCS	t_{CSS}	Chip select setup time (Write)	15	-	ns	-
	t_{CSS}	Chip select setup time (Read)	60	-		
	t_{CSH}	Chip select hold time (Write)	15	-		
	t_{CSH}	Chip select hold time (Read)	65	-		
DNC	t_{AST}	Address setup time	0	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
NWR_SCL (Write)	t_{WC}	Write cycle	66	-	ns	-
	t_{WRH}	Control pulse "H" duration	15	-		
	t_{WRL}	Control pulse "L" duration	15	-		
NWR_SCL (Read)	t_{RC}	Read cycle	150	-	ns	-
	t_{RDH}	Control pulse "H" duration	60	-		
	t_{RDL}	Control pulse "L" duration	60	-		
SDI_SDA (Input)	t_{DS}	Data setup time	10	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DT}	Data hold time	10	-		
SDA, SDO (Output)	t_{RACC}	Read access time	10	50	ns	
	t_{OD}	Output disable time	15	50		

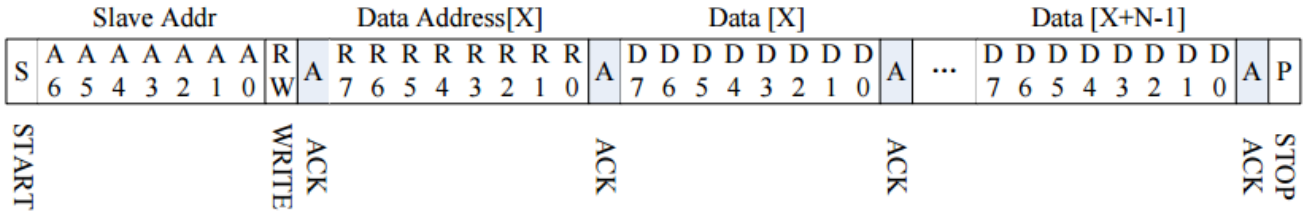
Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Capacitive Touch Panel

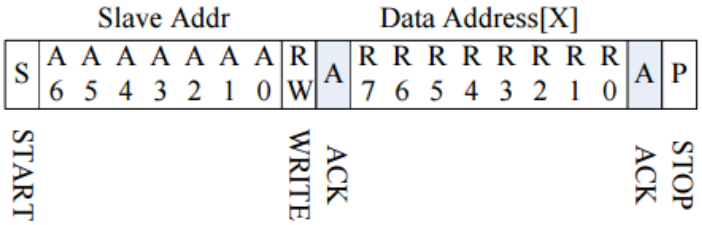


Parameter	Unit	Min	Max
SCL frequency	KHz	0	400
Bus free time between a STOP and START condition	us	4.7	\
Hold time (repeated) START condition	us	4.0	\
Data setup time	ns	250	\
Setup time for a repeated START condition	us	4.7	\
Setup Time for STOP condition	us	4.0	\

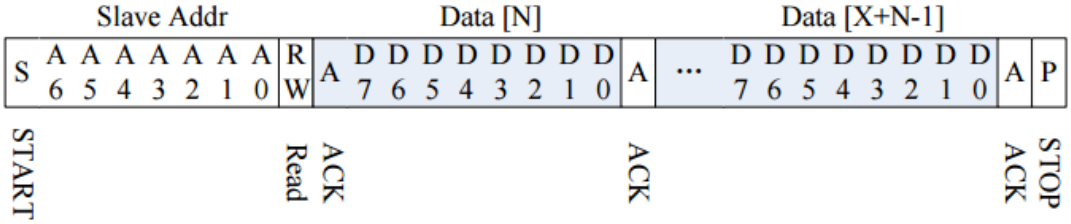
Write N bytes to I2C slave



Set Data Address



Read X bytes from I²C Slave



Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+80°C , 96hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C , 96hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time.	+70°C , 96hrs	2
Low Temperature Operation	Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time.	-20°C , 96hrs	1,2
High Temperature / Humidity Operation	Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time.	+50°C , 90% RH , 96hrs	1,2
Thermal Shock resistance	Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress.	-20°C,60min -> 70°C,60min = 1 cycle, 10 cycles.	
Vibration test	Endurance test applying vibration to simulate transportation and use.	10-50Hz , 1.5mm amplitude. Sweep time: 12min 2 hours in each of 3 directions X,Y,Z	3
Static electricity test	Endurance test applying electric static discharge.	VS=4KV, RS=330Ω, CS=150pF Five times	

Note 1: No condensation to be observed.
Note 2: Conducted after 4 hours of storage at 25°C, 0%RH.
Note 3: Test performed on product itself, not inside a container.

Precautions for using LCDs/LCMs

See Precautions at www.newhavendisplay.com/specs/precautions.pdf

Warranty Information

See Terms & Conditions at http://www.newhavendisplay.com/index.php?main_page=terms